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\*EXAMINER INITIAL

Sheet 1 ATTORNEY DOCKET NO. **FORM PTO-1449** U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE 1687.1005 10/766,955 FIRST NAMED INVENTOR LIST OF REFERENCES CITED BY APPLICANT Hiroyuki YAMASHITA, et al. FILING DATE GROUP ART UNIT (Use several sheets if necessary) January 30, 2004 U.S. PATENT DOCUMENTS

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MR	AC	2000-259445	09/2000	Japan		x				
HR	AD	2001-256072	09/2001	Japan		x				
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HR	AF	Sherwood, Timothy, et al., "Basic Block Distribution Analysis to Find Periodic Behavior and Simulation Points in Applications", International Conference on Parallel Architectures and Complication Techniques", September 2001.		
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HR	АН	Ly, Tai, et al., "Scheduling Using Behavioral Templates", Proc. Design Automation Conf. June 1995.		
HR	AI	Gauthier, Lovic, et al., "Automatic Generation and Targeting of Application Specific Operating Systems and Embedded Systems Software", Proc. Design Automation and Test in Europe, March 2001.		
HR	AJ	Lyonnard, Damien, "Automatic Generation of Application-Specific Architectures for Heterogeneous Multiprocessor System-on-Chip", Proc. Design Automation Conf., June 2001.		

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**FORM PTO-1449** 

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

ATTORNEY DOCKET NO. 1687.1005

APPLICATION NO. 10/766,955

LIST OF REFERENCES CITED BY APPLICANT

FIRST NAMED INVENTOR Hiroyuki YAMASHITA, et al.

(Use several sheets if necessary)

FILING DATE January 30, 2004

GROUP ART UNIT

## **U.S. PATENT DOCUMENTS**

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HR	ВМ	Yoo, Sungjoo, et al., "Automatic Generation of Fast Timed Simulation Models for Operating Systems in SoC Design", Proc. Design Automation and Test in Europe, March 2002.
HR	BN	Ikegami, Kurokawa, et al., "Analysis and Prospects for a C-based Behavioral System LSI Design Flow", IEICE 15th Workshop on Circuits and Systems in Karuzawa, April 22-23, 2002.
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